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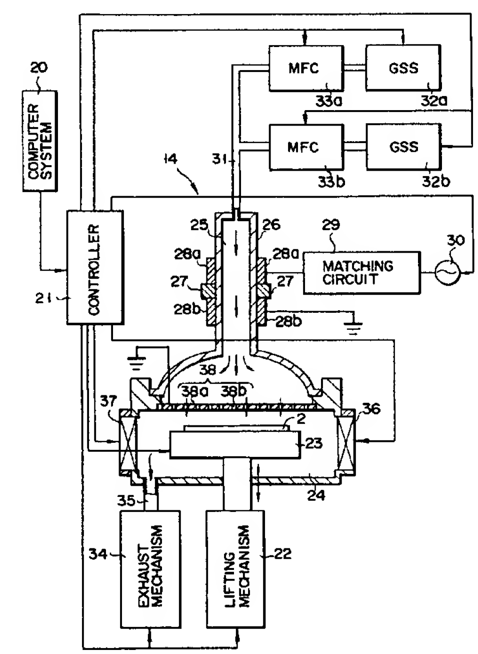
(54) **Apparatus and method for treating substrates.**

(57) A substrates treating apparatus comprising a chamber (14) provided with a section (24) at which a semiconductor wafer (2) is treated and with another section (25) at which plasma is generated, means (32a, 32b, 33a, 33b) for supplying mixed gas (O_2 + CF_4) into the plasma generating section (25) in the chamber (14), high frequency electrodes (28a, 28b) for changing the gas into plasma, an ion trap (38) for trapping ions in the plasma to send neutral radicals into the wafer treating section (24), and means (34) for exhausting the wafer treating section (24).



F I G. 2

EP 0 488 393 A2

The present invention relates to an apparatus for etching and ashing substrates such as semiconductor wafers. It also relates to a method of doing the same.

A micro-pattern of an integrated circuit on a semiconductor is formed by etching an undercoat film on the semiconductor wafer while using an organic high polymer photo-resist film as its mask. The photo-resist film is removed from the surface of the semiconductor wafer after this etching process.

A plasma etching apparatus having an independent unit chamber to the etching process has been used as one of the substrate treating apparatuses.

An ashing apparatus having an independent unit chamber to the ashing process has also been used as one of the substrate treating apparatuses.

A sequence treating apparatus which is a combination of plural treatment units to achieve various functions is now in use. In the case of this sequence treating apparatus, the anisotropic etching is carried out in a main chamber, the isotropic etching (or light etching for removing damage portion of the silicon film) is then carried out in an after-treatment chamber and the ashing is finally carried out in an ashing chamber.

When it is tried to prevent the substrate from being excessively damaged at the isotropic etching and ashing processes, however, it becomes difficult to achieve a high etching rate (or high speed etching) or a high ashing rate (or high speed ashing). Therefore, the so-called batch process by which plural semiconductor wafer are treated at the same time is used to treat the wafers at low plasma current for a long time (of about 1 hour, for example).

On the other hand, it is easy to achieve a high etching rate at the anisotropic etching process because the plasma etching can be carried out using high frequency current. Therefore, the wafers are usually treated one by one.

In the case of the conventional substrate treating apparatus, therefore, the anisotropic etching step, isotropic etching step and the ashing step must be carried out by their corresponding apparatuses and the wafers to be treated must be carried between these apparatuses by hands or by automatic carriage means. This makes it necessary to carry the wafers between these apparatuses and carry them into and out of these apparatuses, thereby making low the throughput to put together the all processes.

In addition, the wafers are contacted with atmosphere while being carried between these apparatuses. This allows dust, impurities and water in atmosphere to adhere to the wafers, thereby creating fault patterns and making the revival of treatment worse. Further, the floor space occupied by the system is increased.

Particularly when the semiconductor wafer is contacted with atmosphere while being carried from the metal etching process to the resist film removing process, a micro-amount of chlorine etching gas remaining on the semiconductor wafer reacts with water in atmosphere to corrode the metal layer on the wafer. If this corroded layer is not removed from the surface of the semiconductor wafer, therefore, the yield of semiconductor device decreases.

An object of the present invention is therefore to provide an apparatus for treating substrates and also to provide a method for doing the same, said apparatus and method being capable of making the treatment speed higher, increasing the throughput, reducing the floor space occupied by the system, and preventing the substrates such as semiconductor wafers from being contaminated by atmosphere.

According to an aspect of the present invention, there can be provided a substrates treating apparatus comprising a chamber provided with a section at which the substrates are treated and with another section at which plasma is generated, means for supplying gas into the plasma generating section, electrode means for changing the gas into plasma in the plasma generating section, an ion trap means arranged between the plasma generating section and the substrates treating section to trap ions in the plasma so as to allow neutral radicals to be introduced into the substrates treating section, and means for exhausting the substrates treating section.

According to an another aspect of the present invention, there can be provided a substrates treating method comprising preparing the substrate at a substrates treating section in a chamber, introducing gas into a plasma generating section in the chamber, changing the gas into plasma in the plasma generating section, taking out neutral radicals from the plasma, and acting the neutral radicals on the substrate in the substrates treating section.

It is preferable that the inner diameter of the plasma generating section is made smaller than that of the substrates processing section. The interval between the electrodes is thus made small to generate plasma of high density. It is preferable that the inner diameter of the plasma generating section is in a range of 20 - 60mm.

Further, it is preferable that a substrate mount is provided with a lifter means to change the interval between the substrate and the ion trap. In this manner it is possible to control the ratio of fluorine radicals allowed to reach the substrate, which are long in life, to oxyger radicals allowed to reach the

substrate, which are short in life.

According to a substrates treating apparatus of the present invention, plasma of high density can be generated and introduced into the substrates treating section through the ion trap to act on the substrate to be treated. Therefore, only radicals are allowed to act on the substrate to be treated, so that the isotropic etching can be carried out at a higher rate without damaging the substrate by ions. Even when the substrates are treated one by one, for example, a throughput in the anisotropic etching can be achieved substantially same in the isotropic etching. The substrates treating section can be connected to a section in which the anisotropic etching apparatus is housed, to thereby treat the substrates one by one while keeping them not contacted with atmosphere.

According to a substrates treating method of the present invention, process gas can be a mixture of ashing and etching gases, the ashing and isotropic etching processes can be carried out at the same time, and the rate of the ashing speed relative to the etching speed can be controlled to a desired value by adjusting at least one of alternative current, the pressure and flow rate of gas and the rate of gases mixed. The ashing and isotropic etching processes can be therefore carried out in a same chamber to thereby make the throughput higher. In addition, the floor space occupied by the system can be reduced because the number of apparatuses used is reduced.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 shows the whole layout of the etching treatment system in which the substrates treating apparatus according to an embodiment of the present invention is included;

Fig. 2 is a block diagram showing the main portion of an after-treatment chamber (ATC) sectioned, which serves as the substrates treating apparatus according to the present invention;

Fig. 3 is a flow chart showing steps of etching and ashing a semiconductor wafer;

Figs. 4A through 4C are vertically-sectioned views showing the semiconductor wafer treated by the etching and ashing steps, respectively;

Fig. 5 is a vertically-sectioned view showing an ion trap and the semiconductor wafer partial and enlarged in order to compare and explain performances of oxygen radicals and fluorine radicals;

Fig. 6 is a graph showing the interrelation of alternative current added to electrodes of a plasma generator means relative to an etching rate (ER), an uniformity (Unif) and a ratio of etching rate/ashing rate (VS. Poly);

Fig. 7 is a graph showing the interrelation of the pressure of process gas relative to the ER, Unif and VS. Poly;

Fig. 8 is a graph showing the interrelation of the flow rate of process gas relative to the ER, Unif and VS. Poly; and

Fig. 9 is a graph showing the interrelation of the rate of CF_4 added to process gas relative to the ER, Unif and VS. Poly.

An embodiment of the present invention will be described with reference to the accompanying drawings.

As shown in Fig. 1, a system 10 for etching and ashing semiconductor wafers comprises plural chamber units 11 - 15. A main chamber (MC) 12 is located between load lock chambers (LLC) 11 and 13 and an after-treatment chamber (ATC) 14 between load lock chambers 13 and 15. Each of the load lock chambers 11, 13 and 15 is provided with a handling device (not shown), by which semiconductor wafers can be carried one by one into and out of the chamber through a gate section (not shown).

A cassette conveying passage (not shown) is arranged adjacent to a front gate of the first load lock chamber 11. A carriage robot (not shown) runs on the cassette conveying passage to convey wafer cassettes from a developing section (not shown) to a cassette station (not shown). The cassette station is located in front of the front gate of the first load lock chamber 11.

Similarly, a cassette station (not shown) is located adjacent to a rear gate of the third load lock chamber 15.

Exhaust and nitrogen gas supply pipes (not shown) are passed through a wall of the load lock chambers 11, 13 and 15, respectively.

A pair of plate electrodes (not shown) parallel to each other are arranged in the main chamber 12 and a Si film on the wafer is anisotropy-etched by plasma generated between the electrodes. Exhaust pipe (not shown) and process gas supply pipe (not shown) are passed through a wall of the main chamber 12.

The after-treatment chamber (ATC) 14 will be described referring to Fig. 2.

A wafer mount 23 which can hold a semiconductor wafer 2 thereon by an electrostatic chuck device, for example, is arranged in the ATC 14. This wafer mount 23 is housed in a treating section 24 which is shaped like a hollow cylinder having a diameter of 200 mm, for example. The wafer mount 23 is moved up and down by a lifter means 22 and it is also provided with a heater (not shown).

A plasma generating section 25 is located above the treating section 24, which is shaped like a hollow cylinder having a diameter smaller than that of the treating section 24. In other words, a

cylindrical tube 26 made of quartz and having a diameter of 40 mm, for example, smaller than that of the treating section 24 is connected to upper portion of the treating section 24. A pair of electrodes 28a and 28b are wound round the quartz-made cylindrical tube 26 with an insulating spacer 27 interposed between them.

One 28a of these electrodes is connected to a high frequency power source 30 via a matching circuit 29 while the other 28b is grounded. A gas supply pipe 31 is connected to the upper end of the cylindrical tube 26 and it is also connected to process gas supply sources (GSS) 32a and 32b through mass flow controllers (MFC) 33a and 33b.

Oxygen gas is contained in the first GSS 32a and CF_4 gas in the second GSS 32b.

An exhaust pipe 35 of an exhaust device 34 is connected to the lower portion of the treating section 24. Gate devices 36 and 37 are arranged on both sides of the treating section 24 to allow the semiconductor wafer 2 to be carried into and out of the treating section 24. The ATC 14 is partitioned from the second and third load lock chambers 13 and 15 by these gate devices 36 and 37.

Further, an ion trap 38 is provided between the treating section 24 and the plasma generating section 25. This ion trap 38 is made by forming a plurality of holes 38b (each having a diameter of 0.2 - 0.5 mm, for example) in a conductive aluminium plate 38a, for example, and it is earthed. Ions in plasma generated at the plasma generating section 25 are caught by the ion trap 38 so as to allow only those radicals which are electrically neutral to act on the semiconductor wafer 2. The ion trap 38 may be a mesh-like electrode.

A controller 21 backed up by a computer 20 is connected to power source switches for the means of the ATC 14. Namely, it is arranged that command signal is sent from the controller 21 to the high frequency power source 30, GSS 32a, 32b, MFC 33a, 33b, lifter device 22, exhaust device 34, gate device 36, 37, electrostatic chuck device, heating device for heating the wafer mount 23 and a wafer handling device (not shown).

The case where the semiconductor wafer 2 is etched and ashed by the etching system 10 will be described referring to Figs. 3 through 5.

The silicon wafer 2 which has been coated with a photo-resist and then developed is taken out from the cassette and carried into the first load lock chamber 11 by the handling device (step 51). The first load lock chamber 11 is closed by its front gate and then exhausted. When the internal pressure of the first load lock chamber 11 becomes substantially same as that of the main chamber 12, the rear gate of the first load lock chamber 11 is opened to communicate the first load lock chamber 11 with the main chamber 12. The wafer 2 is carried from the first load lock chamber 11 into the main chamber 12 (step 52).

Anisotropic etching is applied to the wafer 2 in the main chamber 12 (step 53). A layer 2b of SiO_2 on the wafer 2 is thus partially removed. In other words, the wafer 2 which is under the state shown in Fig. 4A is changed as shown in Fig. 4B. Reference numeral 2a represents the layer of silicon and 2c the layer of photo-resist. That area 3 on the surface of the silicon layer 2a from which the SiO_2 layer has been removed by the anisotropic etching is damaged as shown in Fig. 4B.

The rear gate of the main chamber 12 is then opened and the wafer 2 is carried from the main chamber 12 into the second load lock chamber 13 by the handling device (step 54). The rear gate is closed and the load lock chamber 13 is exhausted until the internal pressure of the second load lock chamber 13 becomes substantially same as that of the ATC 14. The front gate 36 of the ATC 14 is opened and the wafer 2 is carried from the load lock chamber 13 into the ATC 14 by the handling device (step 55). The wafer 2 is fixed on the wafer mount 23 by the electrostatic chuck device. The wafer mount 23 is previously heated to a predetermined temperature or about 50°C, for example.

The wafer mount 23 is lifted by the lifter device 22 and the interval L between the ion trap 38 and the semiconductor wafer 2 is set a predetermined value of 10 - 50 mm, for example, where most ion radicals are present.

Exhausting the treating section 24 through the exhausting device 34 while controlling the flow rate of gas by the MFC 33a and 33b, predetermined process gas such as (O_2 + CF_4) mixed gas is introduced from the gas supply sources 32a and 32b into the plasma generating section 25. At the same time, current having a predetermined high frequency of 1356MHz, for example, is supplied from the high frequency power source 30 to the electrodes 28a and 28b through the matching circuit 29.

Plasma of high density is thus generated in the plasma generating section 25 smaller in diameter than the treating section 24 and this plasma gas is diffused as shown by arrows in Fig. 2. Ions in the plasma gas are removed while it is passing through the ion trap 38, and radicals thus left are supplied to the semiconductor wafer 2 on the wafer mount 23 to conduct the anisotropic etching to the damaged area 3 of the silicon layer 2 and the ashing to the photo-resist layer 2c at the same time (step 56). In order to apply the anisotropic etching and the ashing to the semiconductor wafer 2 to desired extents in this case, it is necessary to control the rate of the etching and the ashing.

The ratio of etching rate/ashing rate (which will be hereinafter referred to as VS. Poly) can be

controlled by adjusting at least one of current added to the electrodes 28a and 28b, the gas flow rate, gas pressure and components of process gas and the interval L.

The reason why the VS. Poly is influenced by the interval L will be described referring to Fig. 5.

When the plasma is passed through the holes 38b of the ion trap 38, ions are removed from it, thereby allowing oxygen radicals and fluorine radicals to reach the wafer 2 in the treating section 24. The oxygen radicals of them react with the photo-resist layer 2c on the wafer 2 to remove the photo-resist layer 2c from the wafer 2 (ashing). On the other hand, the fluorine radicals react with the silicon layer 2a on the wafer 2 to remove the damaged area 3 to a depth of 50 - 100Å (anisotropic etching).

The oxygen radicals are usually shorter in life than the fluorine radicals. When the interval L between the wafer 2 and the ion trap 38 is made too large, therefore, the oxygen radicals become to oxygen gas molecules, so that the photo-resist layer 2c cannot be removed from the wafer 2 because of oxidation reaction. When the interval L is made too small, the speed of anisotropic etching is increased not to set an appropriate light etching rate.

As shown in Fig. 4C when the light etching and ashing treatments are applied to the wafer 2 in the ATC 14, the damaged area 3 and the photo-resist layer 2c are removed from the wafer 2.

The wafer 2 is then carried from the ATC 14 into the third load lock chamber 15 (step 57) and further carried out of the load lock chamber 15 (step 58).

Merits achieved by this embodiment of the present invention will be described referring to Figs. 6 through 9.

An etching rate (ER), an uniformity (Unif) and a ratio of etching rate/ashing rate (VS. Poly) are plotted on vertical axes of graphs shown in Figs. 6 through 9. On the other hand, alternative current is plotted on a horizontal axis of the graph shown in Fig. 6, the pressure of treating gas on a horizontal axis of the graph in Fig. 7, the flow rate of process gas on a horizontal axis of the graph in Fig. 8, and the rate of CF_4 added to the process gas on a horizontal axis of the graph in Fig. 9. Except the case shown in Fig. 8, the total flow volume of CF_4 and O_2 mixed gas is 1250SCCM and except the case shown in Fig. 9, the ratio of process gas comprises O_2 of 90% and CF_4 of 10%.

It is usually needed that the VS. Poly is selected to be 200 - 500.

According to the above-described ATC 14 of the present invention, plasma is generated in the plasma generating section 25 which has a diameter smaller than that of the treating section 24 and it is introduced into the treating section 24 through the ion trap 38 to act on the semiconductor wafer 2 in the section 24. Therefore, it can be generated to have a higher density and it can also be generated at a higher efficiency. The ashing rate at the ashing process can be greater than that of the conventional case (about thirty times of the conventional case), and a throughput (one wafer per minute, for example) same as that at the anisotropic etching can be attained. Further, ions in the plasma can be removed by the ion trap 38 to allow only radicals to be reacted with the semiconductor wafer 2. This enables the isotropic etching to be carried without damaging the semiconductor wafer 2.

Still further, same throughput as that at the anisotropic etching can be attained as described above. This makes it possible to provide a system wherein the main chamber 12 and the ATC 14 are connected to each other by the load lock chamber 13 to carry out the anisotropic and the isotropic etching process successively while carrying the semiconductor wafer 2 not to contact atmosphere. It can be therefore prevented that etching gas of the chlorine group remaining on the semiconductor wafer 2 reacts with water in atmosphere to corrode the metal layer of the wafer 2 at the metal etching process. Therefore, the yield of semiconductor device increases.

Still further, The isotropic etching relative to the silicon layer on the wafer 2 and the ashing relative to the photo-resist layer thereon can be carried out at the same time to thereby increase the throughput. Still further, the ashing device and the carriage means for carrying the wafer between the section at which the isotropic etching treatment is carried out and the section at which the ashing treatment is carried out are made unnecessary to thereby reduce the floor space occupied by the system. The space particularly in a clean room whose constructing cost is high can be more efficiently used.

Although AC has been used as the plasma power source in the case of the above-described embodiment, the present invention is not limited to AC but DC may be used.

According to the above-described apparatus and method for treating substrates, the treating speed can be made higher at the isotropic etching and ashing processes to thereby increase the throughput. In addition, the floor space occupied by the system can be reduced and treatments can be carried out while keeping the wafer not contacted with atmosphere.

Claims

1. A substrates treating apparatus comprising

a chamber (14) provided with a section (24) at which the substrate (2) is treated and

with another section (25) at which plasma is generated;

gas supplying means (32a, 32b, 33a, 33b) for supplying gas into the plasma generating section (25);

electrode means (28a, 28b, 29, 30) for changing the gas into plasma in the plasma generating section (25);

ion trap means (38) arranged between the plasma generating section (25) and the substrate treating section (24) to trap ions in the plasma so as to send neutral radicals into the substrate treating section (24); and

exhausting means (34) for exhausting the substrate treating section (24).

2. The substrates treating apparatus according to claim 1, characterized in that the diameter of the plasma generating section (25) is smaller than that of the substrate treating section (24).

3. The substrates treating apparatus according to claim 1, characterized in that the plasma generating section (25) is located above the substrate treating section (24).

4. The substrates treating apparatus according to claim 1, characterized in that the substrate in the substrate treating section (24) is opposed to the ion trap means (38).

5. The substrates treating apparatus according to claim 4, characterized by further comprising interval changing means (22) for changing the interval between the substrate in the substrate treating section (24) and the ion trap means (38).

6. The substrates treating apparatus according to claim 1, characterized in that the electrode means (28a, 28b, 29, 30) includes a first electrode (28a) connected to a high frequency power source, and a second electrode (28b) insulated from the first electrode (28a) and grounded.

7. The substrates treating apparatus according to claim 1, characterized in that the ion trap means (38) has a porous metal plate grounded.

8. The substrates treating apparatus according to claim 1, characterized in that the gas is a mixed one including oxygen and fluorine.

9. The substrates treating apparatus according to claim 1, characterized by further comprising a means (23) for heating the substrate in the substrate treating section (24).

10. A substrates treating method comprising

preparing a substrate (2) in a substrate treating section (24) of a chamber (14);

introducing gas into a plasma generating section (25) in the chamber;

changing the gas into plasma in the plasma generating section (25);

taking out neutral radicals from the plasma; and

acting the neutral radicals on the substrate (2) in the substrate treating section (24) whereby carrying out isotropic etching and ashing relative to the substrate (2) at the same time.

11. The substrates treating method according to claim 10, characterized in that at least one of the flow rate, pressure and components of the gas is controlled to control a ratio of the ashing rate and the isotropic etching rate.

12. The substrates treating method according to claim 10, characterized in that the amount of plasma generated is adjusted to control a ratio of the ashing rate and the isotropic etching rate.

13. The substrates treating method according to claim 10, characterized in that the interval between the means (38) for taking out the neutral radicals from the plasma and the substrate (2) is adjusted to control a ratio of the ashing rate and the isotropic etching rate.

14. The substrates treating method according to claim 10, characterized in that the ashing rate is controlled to be range of 200 - 500 times of the isotropic etching rate.

15. The substrates treating method according to claim 10, characterized by further comprising the step of heating the substrate during to generate the plasma.

16. The substrates treating method according to claim 10, characterized in that the gas is a mixed one including oxygen and fluorine.

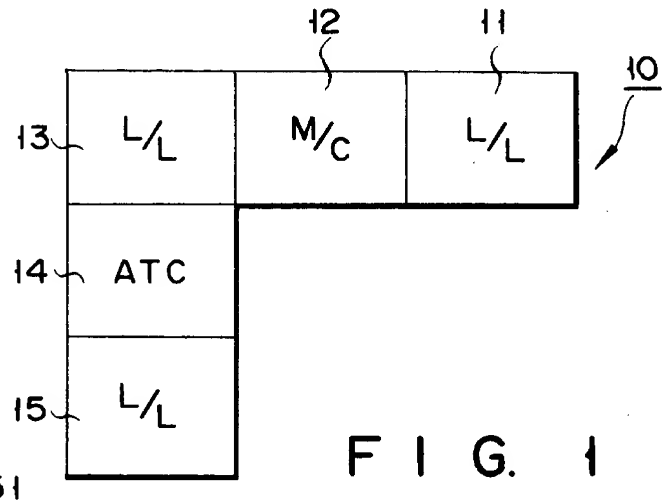


FIG. 1

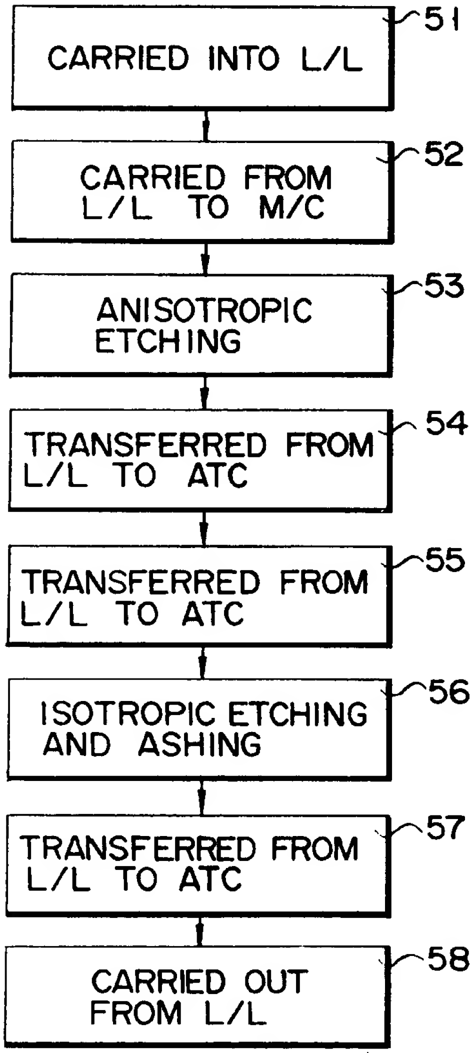


FIG. 3

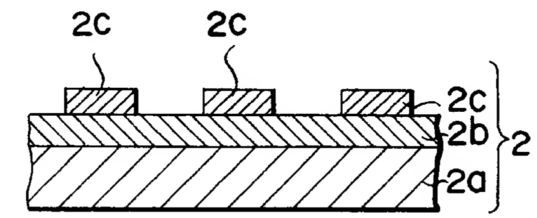


FIG. 4A

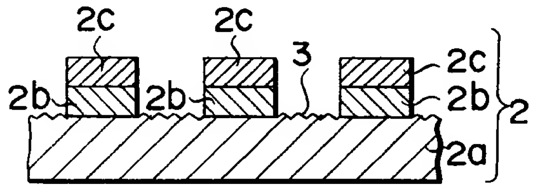


FIG. 4B

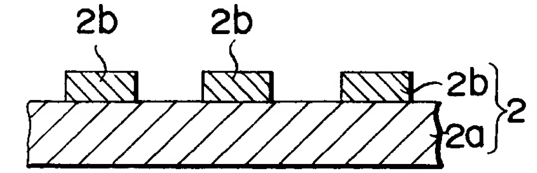
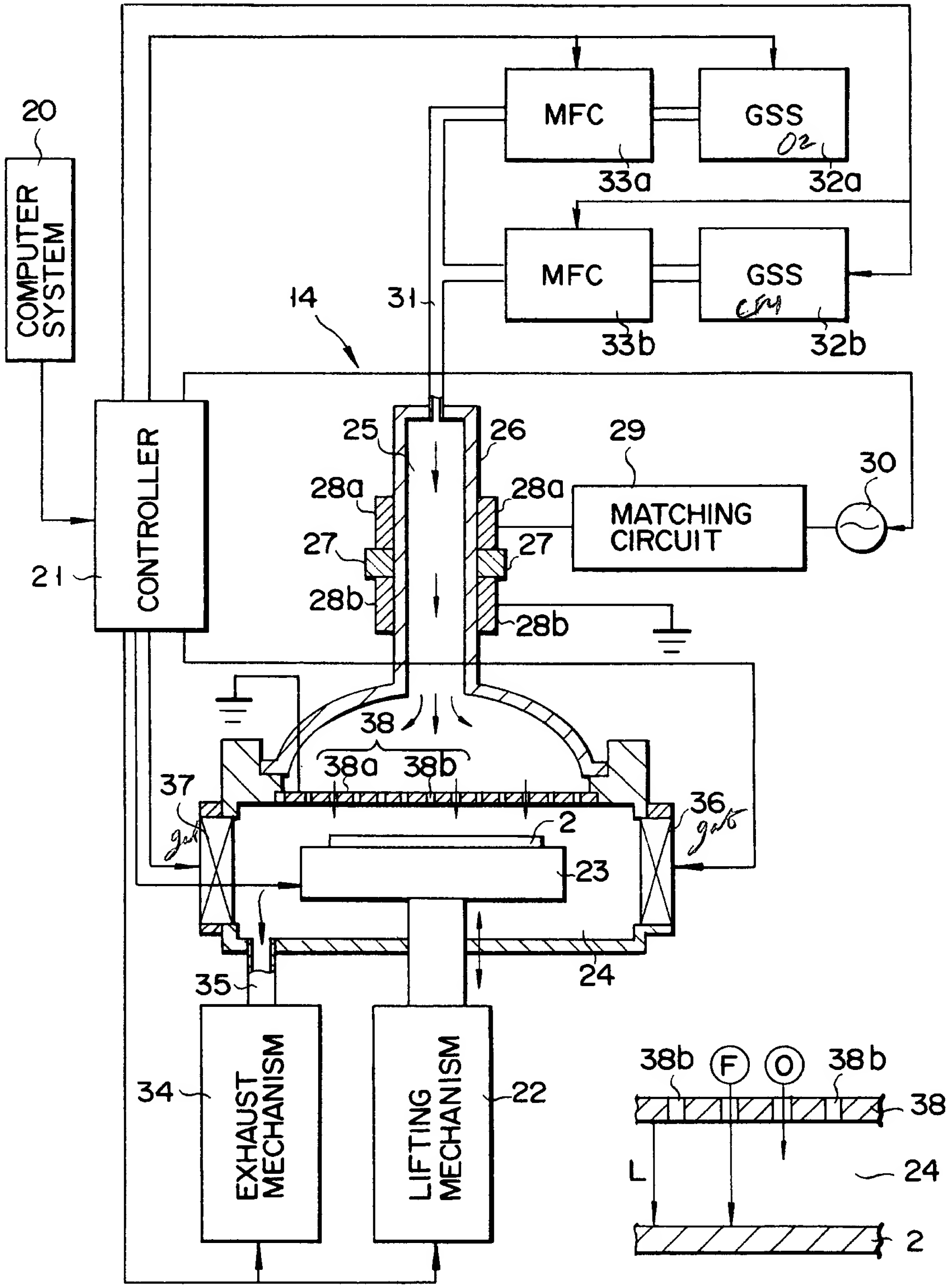
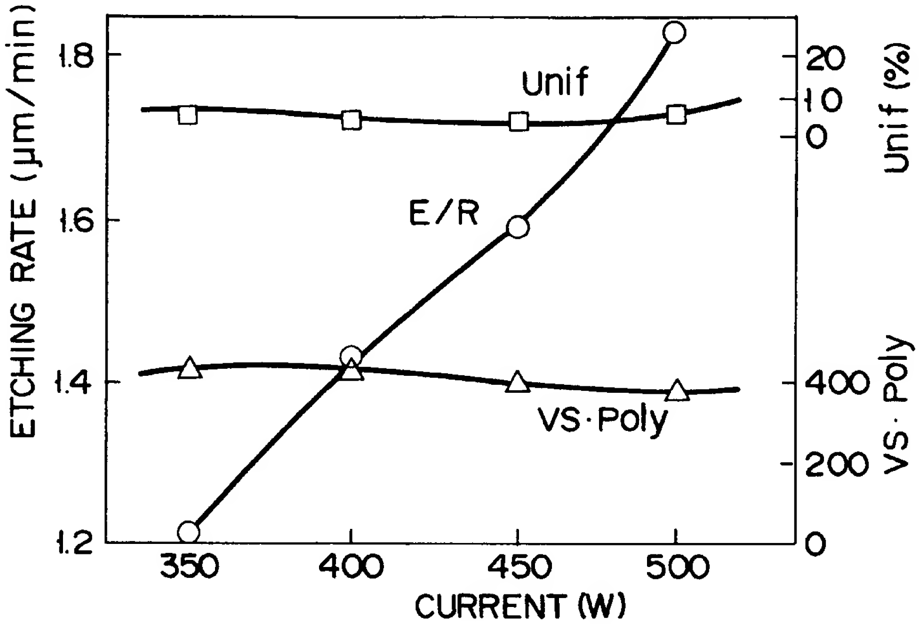


FIG. 4C

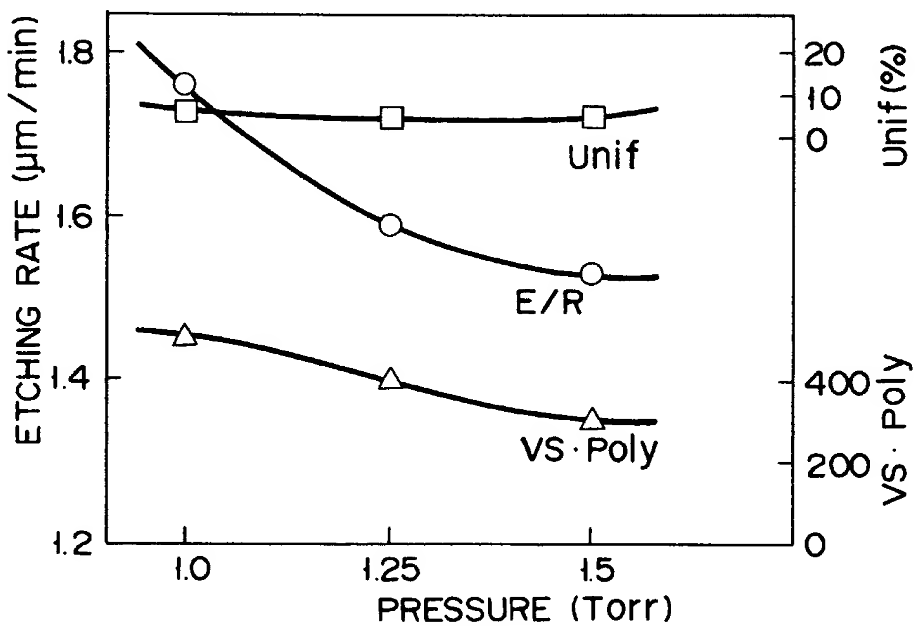

MFC
GSS
O2
33a
32a
MFC
GSS
CF4
33b
32b
20
COMPUTER SYSTEM
14
31
CONTROLLER
21
25
26
29
30
28a
28a
MATCHING CIRCUIT
27
27
28b
28b
38
38a
38b
37
gate
36
gate
2
23
24
35
EXHAUST MECHANISM
34
LIFTING MECHANISM
22
38b
F
O
38b
38
L
24
2

F I G. 5

F I G. 2


ETCHING RATE (μm/min)
1.8
1.6
1.4
1.2
Unif
E/R
VS·Poly
20
10
0
400
200
0
Unif (%)
VS·Poly
350
400
450
500
CURRENT (W)

F I G. 6


ETCHING RATE (μm/min)
1.8
1.6
1.4
1.2
Unif
E/R
VS·Poly
20
10
0
400
200
0
Unif (%)
VS·Poly
1.0
1.25
1.5
PRESSURE (Torr)

F I G. 7

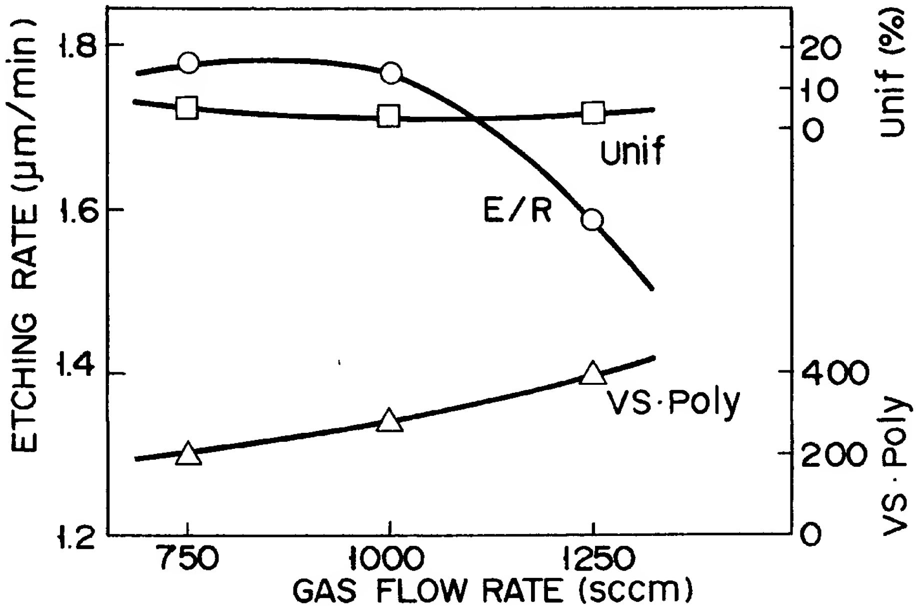

ETCHING RATE (μm/min)
1.8
1.6
1.4
1.2
750
1000
1250
GAS FLOW RATE (sccm)
Unif (%)
20
10
0
400
200
0
VS·Poly
Unif
E/R
VS·Poly

FIG. 8

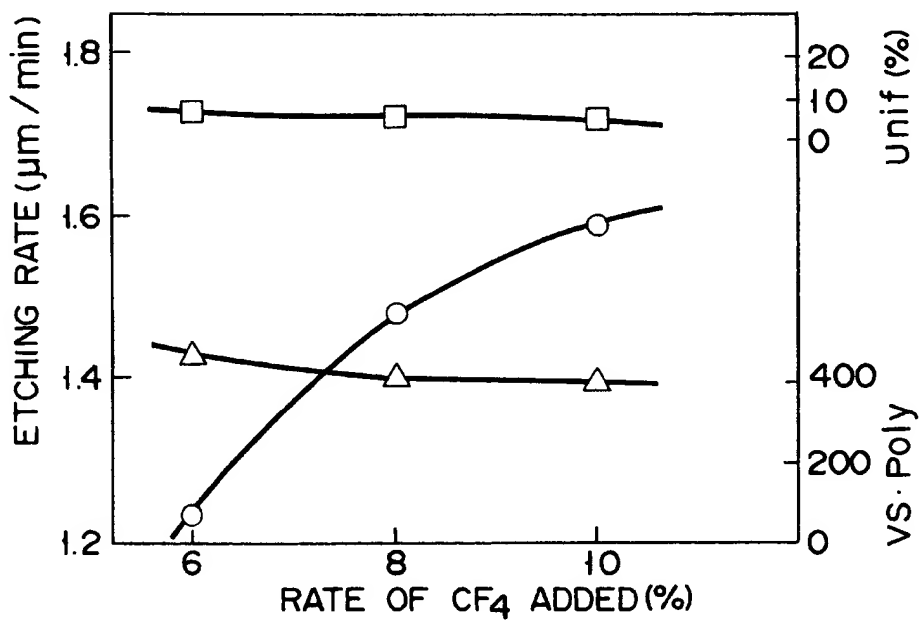

ETCHING RATE (μm / min)
1.8
1.6
1.4
1.2
6
8
10
RATE OF CF4 ADDED (%)
Unif (%)
20
10
0
400
200
0
VS·Poly

FIG. 9